

INFSO

Embedded Systems Design Workshop

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••• **An assessment of four years of funded research
on Embedded Systems Design**



Table of Contents

EXECUTIVE SUMMARY	4
Introduction	4
Key Results	4
Background	6
What are embedded systems?	6
R&D Expenditure in Embedded Systems	7
Programme Objectives	8
Project Presentations	9
Recent and forthcoming calls for proposals	17
FP7 Call 1, objective 3.3, Embedded Systems Design, Budget: 40 M€	17
ARTEMIS Joint Undertaking	17
FP7 ICT Target outcomes WP '09-10, Objective 3.4 (Budget 28 M€) :	17
Discussion of the presentations	18
Discussion of the presentation of the Network of Excellence	18
Discussion of the presentations of the Integrated Projects	19
Discussion of the presentations of the STREP Projects	19
Conclusions and Recommendations	20
Conclusions	20
Recommendations	21
Annex A: References	22
Annex B: Attendees and Agenda	23

EXECUTIVE SUMMARY

Introduction

Embedded Systems are an acknowledged strength of European industry. In recent years improvements have been made in the productivity and efficiency of the development of Embedded Systems as a result of constant efforts to improve design methodologies and their supporting tools. The scope of the term Embedded System covers a huge range of products from consumer electronics through automotive systems to extremely complex aerospace systems.

The wide scope of products that contain Embedded Systems and the very different regulatory regimes applied across the product types discourage the cohesion of this large group of designers. Embedded System design and development is normally taught as an adjunct to another engineering course. These factors contribute to the feeling expressed by Embedded System designers that whilst they participate in a multi billion € industry, it is fragmented and sandwiched between hardware and software design. An integrated set of development methods and tools is lacking in Embedded Systems.

The continuing emergence of new markets for intelligent devices in ubiquitous computing as applied to the domestic, medical, automotive and aerospace sectors offers the opportunity for Europe to maintain and enhance its strength in Embedded Systems. However for Europe to retain its pre-eminent position in Embedded Systems a sustained programme of research and development in design methods for Embedded Systems and a cultural change from being considered, largely, a craft based process to becoming a science based industrial process is needed. To this end, the FP6 & FP7 R&D support programmes and the creation of the ARTEMIS technology platform and its supporting association, ARTEMISIA, have begun to create an identity and a focus to bring about the required cultural and methodological changes in the European community of Embedded Systems designers and developers.

The objective of the workshop was to take stock of the recent work on Embedded System Design in FP6 projects. 3 Integrated Projects, 5 Specific Targeted Research Projects (STREP) and 1 Network of Excellence were launched in response to the 2003 call 2 for proposals. These projects presented the results obtained and these were assessed with respect to the project objectives and the overall objectives set out within the FP6 Workplan. Consideration was given to the lessons learned, the successful prototyping of new methods, the expected impact of the results, both within the project partnership and through the external exploitation of results and new business generated.

Key Results

The results presented showed that there has been excellent progress in the 3 Integrated projects working on the development of end-to-end tool flows from the different viewpoints of Proof Based Design of Embedded Systems, design of Time Triggered systems and systems based on Resource Contract relationships. Each system had been developed to meet the needs of the partners in different industrial sectors and clearly demonstrate the range of solutions needed to efficiently fulfil the requirements of different industrial sectors. The STREP projects have made good progress with domain specific tools that have been demonstrated to have benefit to the design problems concerned. These developments have good potential for exploitation by the participants in the project and to the wider user base through tool vendor partners within the consortium.

The Network of Excellence has attracted the leading researchers in the field and made good progress to create a community infrastructure and structure the scientific agenda for Embedded Systems research.

In summary the projects' achievements are:

ARTIST2 - The project has created a European Embedded Systems community with a global standing, an incubator for research projects and undertaken important work toward developing Embedded Systems as an education discipline.

ASSERT - This project has developed a proof-based design method with supporting tools which covers all the phases of an embedded system design from early system definition down to final code while preserving properties.

DECOS - The partners have produced and validated a time triggered platform design to reduce complexity, increase dependability, reduce hardware cost (up to -10%), with easy integration of new functions and different suppliers IP. The platform can deliver improved diagnosis which leads to

reduced Maintenance Cost (-20%) and reduced cost for validation and certification (-25%). The tool chain from DECOS is forecast to reduce development cost (up to -20%) when the tools are industrialised.

SPEEDS - The project aims to produce a formal methodology to enable concurrent engineering of complex embedded systems. A new specification language for the expression of “contracts” (CSL) has been defined. The main objectives of CSL are to enable full-scale reuse of components and to secure concurrent design processes, while enabling the assessment of design maturity at any stage of the project using the concept of “contracts” defining function and performance between the sub-systems.

HIJA - The HIJA project has provided embedded systems developers the capability of dynamic deployment and code portability in high integrity systems.

ICODES - The advantages of the ICODES design flow stem from raising the level of abstraction to transaction level modelling of the high level design elements both hardware and software that make up embedded systems.

COMPARE - The project has provided a definition of a RT/E framework based on Lightweight-CCM (Component/Container Model) with a reference implementation on top of RTCORBA.

INTEREST - The project aims to create techniques for improved interoperability among European Embedded Systems Design, code generation, and verification COTS (commercial off the shelf) tools.

VERTIGO - The technologies investigated in VERTIGO have improved the performance of an industry design flow through the successful integration of innovative technologies from the EDA tools developed by the SME partners.

The results from the workshop will contribute to a fuller understanding of what has been achieved and what needs to be achieved in the planning of future actions. This workshop highlighted the value of supporting work in this area and provides a base for future programmes of project support.

The success of this workshop has prompted the idea to repeat the format in early 2009 with participation of FP7 Call 1 running projects, new projects from call 2 and future calls.

Background

The embedded systems sector is today one of the pillars of European industrial development. Over recent years improvements have been made in the productivity and efficiency of their development as a result of constantly improved design methodologies and tools for model based design. Two points have to be emphasized: firstly the need for increased industrial efficiency continues to be at the heart of international competitiveness; secondly model based design and its supporting tools are one of the most significant, improvements. Tools proliferate and improve selected sections of the process but lack of connectivity and of a common sound semantic foundation has limited, in practice, the productivity gains that can be obtained. These issues are compounded by the speed of technological evolution over recent years that have led to a need for radical change in Embedded System design. The use of new technologies at silicon level implies huge NRE (Non-Recurrent Engineering) costs, and the amortisation of these NRE costs in turn requires huge volumes. Platform-based approaches can facilitate such high volumes.

What are embedded systems?

Embedded systems are special-purpose computer systems designed to perform *one or a few dedicated functions*, often with *physical and operational constraints* such as limited memory or processing capacity, low-power consumption, real-time behaviour, high dependability, etc. They are often (but not always) hidden in everyday devices from mobile phones and home appliances to cars and planes. The purpose of these *computers that do not look like computers* is to control and enhance the functionalities of the equipments where they are embedded into. In contrast, a general-purpose computer, such as a personal computer, can do many different tasks, depending on programming, and in most cases do not operate under such stringent constraints.

Systems design is the process of deriving, from requirements, a model from which a system can be generated more or less automatically. A model is an abstract representation of a system. For example, software design is the process of deriving a program that can be compiled; hardware design, the process of deriving a hardware description from which a circuit can be synthesized. In both domains, the design process usually mixes bottom-up and top-down activities - the reuse and adaptation of existing component models and the successive refinement of architectural models in order to meet the given requirements. [Henzinger & Sifakis]

Building embedded systems of guaranteed functionality and quality, at an acceptable cost, is a major technological and scientific challenge. The challenge to researchers and designers is to produce theoretical and practical methods and tools, which allow system oriented design approaches, to achieve high optimisation of the overall product for its intended market segment; encompassing cost, time to market, quality, safety, security, reliability, dependability and use of resources (energy, bandwidth, processor, memory, etc)

There is almost no industrial sector not integrating Embedded Systems: automotive or aerospace, industrial automation or medical/healthcare, telecommunication or consumer electronics, or many others. Embedded Systems have a deep impact on these industries and on the final consumer of their products as well.

Embedded Systems are the key to innovation. Innovative products might become a commodity, as everyone in the global market can produce them. At the commodity level, the consumer will no longer select just by quality or functionality, but also by price. However, the speed of innovation is a key differentiator that can lead to a successful market leadership. Time to market is one essential factor for innovative products. Supporting tools and methods can significantly reduce the design time. Europe cannot compete for commodity products but has to look into innovation constantly, and bring new products into the market in shorter and shorter time.

The progress of the semiconductor industry has made it economically feasible to replace mechanical and hydraulic control systems by embedded computer systems and to increase their functionality far beyond the capabilities of the systems they replace. The automotive industry shares the view that in the next 10 years 90% of its expected innovations will be based on novel IT applications within the car and its environment.

R&D Expenditure in Embedded Systems

In Billion Euros

	2003		2009	
	Total ICT R&D	of which ES R&D	Total ICT R&D	of which ES R&D
EU25	21.7	12.1 (56%)	34.6	22.9 (66%)
US	68.0	28.3 (42%)	103.2	54.9 (53%)
Japan	24.8	15.4 (62%)	40.7	29.3 (72%)
Rest of Asia	14.2	7.6 (54%)	23.1	15.2 (66%)
World	128.7	63.4 (49%)	201.6	122.3 (61%)

[Source data, FAST]

Assuming the forecasts shown in the tables above prove to be accurate then for Europe to retain it's pre-eminent position in Embedded Systems, investment in a sustained programme of research and development in design methods for Embedded Systems and in education to bring about the cultural change from Embedded System design being considered largely a craft based process to becoming a science based industrial process is needed. To this end, the FP6 & FP7 R&D support programmes and the creation of the ARTEMIS technology platform and its supporting association ARTEMISIA, have begun to create an identity and a focus to bring about the cultural and methodological changes in the community of Embedded Systems.

The ARTEMIS strategic research agenda estimates the worldwide population of Embedded Systems developers to be 460,000 in 2005, growing to 530,000 in 2007 at the start of FP7. Keeping the same growth rate (10 %/year), the Embedded Systems R&D population is therefore expected to double over the next 10 years. [FAST]

Comparing the number of researchers per 1.000 in the labour force, however, the European Union is with 5.8 far behind Japan (10.4 in 2003), the United States (9.2 in 1999) and is just above the average of all OECD countries (5.5). The percentage of Chinese researchers in the labour force is with 1.2 in 2003 the lowest, but it is expected that the absolute number of Chinese science and engineering doctorates awarded will surpass those earned in the United States by 2010. [FAST, p. 107]

Programme Objectives

In the following paragraphs the Embedded Systems objective is reported although this report will concentrate only on the Embedded Systems Design aspects of the objective.

The objective 2.3.2.5 Embedded Systems from the IST WP 2003-2004, [IST-WP0304] and subsequent workplans were to develop the next generation of technologies and tools for modelling, design, implementation and operation of hardware/software systems embedded in intelligent devices. An end-to-end systems vision was required to allow the build of cost-efficient systems with optimal performance, high confidence, reduced time to market and faster deployment.

Projects were required to focus on:

- Middleware and platforms for building Networked Embedded Systems that aim to hide the complexity of underlying computing, communications, sensing and control while, at the same time, providing efficient and effective distribution of resources at low cost. Emphasis was to be on middleware for small wireless devices, e.g. mobile phones or PDAs, that makes design, programming, verification and maintenance of systems including such devices easier. It was also to be on scalable and self-organising platforms that offer services for ad-hoc networking of very small devices and for mastering complexity through perception techniques for object and event recognition and advanced computing and control.
- Concepts, methods and tools for system design, development of warrantable software components and implementation of systems, with emphasis on correct handling of complex Real-Time constraints. Work included unification of computational models and composition methods, holistic design addressing event and time constraints, interface technologies in hard- and software addressing real-world and legacy issues, techniques and integrated validation tools to ensure ultra-stable, dependable embedded systems.
- Advanced Controls for Real-Time systems with emphasis on hybrid systems theories including non-linear processes with both constraints and switching modes. Advanced controls for Networked Embedded Systems with emphasis on networked autonomous and fault adaptive control and management, as well as on reasoning, behaviour, global performance and robustness.

It was expected that work on Networked Embedded Systems and on system design would crystallise around Integrated Projects that also address the relevant parts of work on Advanced Controls. These Integrated Projects were expected to create critical mass by covering: basic and foundational research (e.g. methods, models, languages), component-based research (e.g. new generation of tools) and systems integration. Projects were required to stimulate innovation in business and industrial systems by incorporating leading-edge users with visionary application problems and also users with mid-term issues and SMEs to ensure a wider take-up. An incremental approach starting with a group of core partners was recommended.

Networks of Excellence were expected to complement the Integrated Projects, in particular for Advanced Controls where activities with a longer-term horizon were needed for further structuring the European Research Agenda in this field. Specific Targeted Research Projects and Specific Support Actions were encouraged to explore emerging technologies or alternative approaches so as to pave the way for additional new technological advances in the field.

The aim of this evaluation workshop was:

- to provide feedback on how the programme objectives have been realised,
- to use evaluation results to adjust programmes and to find out the relevance of the programme..

Project Presentations

ARTIST2

NoE, Project dates: Start 09/04 End 09/08

Introduction

The strategic objective of the ARTIST2 Network of Excellence, and its precursor project ARTIST, was to strengthen European research in Embedded Systems Design and promote the emergence of this new multi-disciplinary area as a new education discipline in its own right. The project gathers together the best European teams from the composing disciplines of electrical engineering, computer science, applied mathematics, and control theory. This was achieved by integrating teams and competencies from 7 essential topics called clusters: Modelling and Components, Hard Real-Time, Adaptive Real-Time, Compilers and Timing Analysis, Execution Platforms, Control for Embedded Systems, Testing and Verification. The NoE acts as a Virtual Centre of Excellence in the area of Embedded Systems Design.

Integration is achieved around a Joint Programme of Activities (JPA), aiming to create critical mass from the selected European teams. This interdisciplinary effort in research aims to establish Embedded Systems Design as a discipline, combining competencies from electrical engineering, computer science, applied mathematics, and control theory. The ambition is to compete on the same level as equivalent centres in the USA (Berkeley, Stanford, MIT, Carnegie Mellon), for both the production and transfer of knowledge and competencies, and for the impact on industrial innovation.

Objectives

The goal of ARTIST2 is to integrate joint research activities at two levels within and between topic clusters to create the multi-disciplinary community that will guide the Embedded Systems Design area. Currently, efforts in the area are fragmented, and no single European research group gathers sufficient critical mass. Integrating the clusters is the first step towards integrating the area as a whole.

Results

ARTIST2 has achieved a structuring effect on European research in a variety of respects:

1. The integration of academic research has brought forward new, coherent theoretical frameworks, particularly those that contribute to the unification of the area.
2. ARTIST2 has created a context, an infrastructure and a culture for the design of joint, multi-organisational, multi-disciplinary R&D work in Embedded Systems Design.
3. ARTIST2 aimed to have structural impact on European education in Embedded Systems Design, by:
 - The integration of state of the art knowledge into the curricula and accelerating convergence towards multi-disciplinary approaches.
 - Promoting approaches and techniques, which are well-adapted to meeting current and future industrial needs. The Industrial Advisory Board's input and advice has been essential for this.

The project presented their view of the factors they believe facilitated their success. They maintained tight control of the technical area to be covered and of the quality of the partners based on research excellence, industrial impact and commitment. In order to achieve the critical mass of expertise needed to cover all aspects of Embedded System Design, the size of the consortium was large. Early recognition and active response to the problems of managing large consortia has contributed to the success of this NoE. The project management team introduced active management controls for reporting and both internal and external communication. The project understood that dissemination is a key tool for success and put in place an efficient and active management of the project website, an active programme of events, and a proactive approach to scientific publication and regular mailing of newsletters to an actively managed mailing list of partners, collaborators and interested parties.

ARTIST2 has created a strong 'brand recognition' within the European and international community. This is visible through an excellent dissemination activity and active participation in WG for the ARTEMIS Strategic Research Agenda. The NoE has organised major conferences (Embedded Systems Week, Date, RTSS...) and has been notably successful in peer reviewed IEEE and the ACM papers and publications. ARTIST2 has driven a number of international collaboration activities (high-level meetings and schools). ARTIST2 has been active in triggering important R&D projects (National (A, DK, S) and European). The first FP7 call has been very successful. The following STREP projects have been approved. These projects have a strong involvement from ARTIST2 partners.

- ACTORS - Adaptivity and Control of Resources in Embedded Systems

- ALL-TIMES - Integrating European Timing Analysis Technology
- COMBEST - COMponent-Based Embedded Systems Design Techniques
- EMUCO - Embedded Multi-Core
- JEOPARD - Java Environment for Parallel Real-time Development
- MNEMEE - Memory management technology for adaptive and efficient design of ES
- PREDATOR - Design for Predictability and Efficiency
- Quasimodo - Quantitative System Properties in Model-Driven Design of ES

Many teams from ARTIST2 play a leading role in their own countries, by participating in setting up and leading national centres of excellence and national projects. The European embedded systems community is now becoming a reality, as demonstrated by a strong presence as a community in conferences, and significant interaction between the members at all levels.

The successes of ARTIST and ARTIST2 are being carried forward in the FP7 call 1 ArtistDesign.

ASSERT

Automated proof-based System and Software Engineering for Real-Time applications.

IP, Project dates: Start 09/04 End 12/07

Introduction.

The ASSERT project began from the state of the art where any system is a black box whose properties cannot be fully evaluated although some properties can be extracted from this black box through testing. The consequences of this are that nobody can guarantee the system properties. Confidence in the system can only be increased by testing, (coverage level of tests increases confidence level), but testing cost >50% of development cost. A S/W development can be started even when no solution exists for a given problem. Trying to build software for either complex or unsolvable problems leads to failure.

Studies have shown that the software productivity gap will still increase for the foreseeable future. The project responses to this issue rely on:

- Reducing the cost of system design failures, by enforcing a proof based system component approach, where design solutions are proven "correct by construction".
- Reducing the cost of test and integration.

ASSERT has developed proof-based solutions for these major issues:

- System families supported by proven reference architectures and standardised building blocks.
- A proof-based method encompassing the full system and software lifecycle and supported by a well-defined and automated process.

The project organized into 3 development topic clusters:

- The DDHRT (Dependability, Distribution, Hard Real-Time) cluster in charge of developing the technologies that guarantees the preservation of system properties.
- The DVT (Development and Verification Tools) cluster in charge of developing the modelling and verification techniques to support the ASSERT process.
- The SeMV (System Modelling and Verification) to develop the system modelling technologies to model and verify high level system properties.

These activities were supported by the P&S (Process and Standardisation) cluster in charge of capturing the ASSERT process and identifying the potential impacts to the existing standards and the O&E (Openness and Exploitation) cluster which was responsible for training people to the new technologies and disseminating the project outcomes.

Results

The results from the ASSERT project cover:

- The ASSERT proof-based process:
 - Developed as a result of a consensus within the project
 - Integrates the different technologies used in ASSERT
 - Has shown its scalability and independence w.r.t. the technologies (fully implemented on the ESA demonstrator)

This process is covering all the phases from early system definition down to final code while preserving properties. It has been defined and implemented by integrating tools coming from the technology clusters. It has been exercised and assessed by industrial case studies showing its flexibility and scalability. It will be the basis for dissemination to industrial projects. It will

be extended by a tighter integration of existing technologies and development of new ones in the follow-up actions after ASSERT

- The tools:
 - Some tools have been specifically developed for ASSERT (Tools to support data modelling)
 - Other tools have been developed as extensions or new versions of existing tools.

ASSERT proved the validity of its new concepts by demonstration on real industrial cases, an intensive education and training program and diffusion of the results within a network of industrial partners.

- Satellites on-board SW with THALES ALENIA SPACE,
- Multi-platform and highly available systems with ASTRUM.
- ESA demonstrator where the ASSERT full process has been implemented in 3 months by a team from outside the project.

DECOS¹

Dependable Embedded COmponents and Systems

IP, Project dates: Start 07/04 End 12/07

Introduction.

Historically, the development of computing systems to support safety-critical real-time computer applications (nuclear, aerospace, railway, etc.) has often resulted in a customized solution design approach. This has led to the reinvention of system design concepts, middleware and to limited reuse of code. Summing this across the many and diverse application domains it has exacerbated the extensive costs of verifying and validating complex one-of-a-kind safety critical systems. With the anticipated deployment of time triggered safety-critical systems in many more application domains (automotive, medical, process control, etc.) the availability of a component-based methodology for the cost-effective design, implementation, validation, and certification of integrated dependable embedded systems becomes instrumental for the competitiveness of the European economy.

Objectives

The DECOS project investigates and develops approaches to significantly alleviate the five key obstacles to the rapid and economic deployment of advanced electronic functions in embedded systems i.e. Electronic Hardware Cost, Diagnosis and Maintenance, Dependability, Development Cost, Intellectual Property (IP) Protection. The intent of DECOS was to provide an integrated distributed execution platform, a set of pre-validated *hardware components* and *software modules* and tools for the design of dependable embedded systems. System design approaches that are applicable to diverse application domains were considered. The project targeted automotive, aerospace, railway and control applications.

Results

DECOS provides the basic enabling technology to move from a federated distributed architecture to an integrated distributed architecture, i.e. an execution platform that allows tight integration of software modules from different sources (vendors) and with different criticality levels. This execution platform is supported by methods and tools for system design, a diagnostics infrastructure and software and hardware components based on FPGAs. In order to be able to thoroughly test dependable embedded systems, a test-bench comprising methods and tools for validation and modular certification was created.

Concepts and methodologies to visualise and navigate complex real-world systems during design and validation were developed in order to support design comprehension. Application development is simplified by the provision of basic software building blocks to ease the generation of safe software modules. The applicability of these technologies was shown via demonstrator systems out of three application domains – automotive, aerospace and industrial control. The application of the DECOS methodology is claimed to result in cost reductions in the design and deployment of embedded systems as well as in system hardware cost, maintenance and system development.

Key results achieved by the DECOS partners in:

- System Architecture with Time-Triggered Core Services:
 - Deterministic and Timely Message Transport
 - Fault-Tolerant Clock Synchronisation

¹ According to the dissemination policy of DECOS there is no direct hyperlink to this project's presentation materials. Please refer to the [project's website](#) for more information.

- Strong Fault Isolation
 - Consistent Diagnosis of Failing Nodes
- Model-based Tool-chain with Complete code generation
 - Validation & Verification Framework with Test Guidance and Certification support
 - Door to Future with Time-triggered Ethernet and DECOS Time-triggered, fault-tolerant platform-on-Chip. Proof of Concept has been shown by industrial demonstrators, Electronic Outer Flap Control, Vibration Control for Nano Imprinting Machines and a demonstrator of Driver Assistance Subsystems with Traffic Jam Assistant, Adaptive Lighting and Door Control Systems.

SPEEDS

SPEculative and **EX**ploratory **D**esign in **S**ystems engineering

IP, Project dates: Start 05/06 End 10/09

Objectives

To define a new generation of end-to-end methodologies processes and supporting tools for safety-critical embedded system design. The aim is to evolve from model-based design of hardware/software systems, towards integrated component based construction of complete virtual system models.

The technical approach is a semantics-based modelling method to support the construction of complex embedded systems by composition of heterogeneous subsystems to be enabled by integration of new and existing tools. This modelling approach defines “heterogeneous rich-component” models to represent both functional and non-functional aspects so that efficient implementations can be derived from abstract models.

Novel formal analysis tools and techniques will be used to assess properties of the system that will allow the exploration of architectural alternatives of implementation platforms and enable correct-by-construction designs. Controlled speculative design is a new tool-supported process that minimises the risk of concurrent design activities by establishing formal “contracts” between design groups. A new specification language for the expression of “contracts” (CSL) has been defined. The main objectives of CSL are to develop a framework for multiple component viewpoints (functional and non-functional, discrete and continuous), to enable full-scale reuse of components and to secure concurrent design processes, while enabling the assessment of design maturity at any stage of the project using the concept of “contracts” between components

SPEEDS promises a significant reduction of development costs and a reduction of development time for safety-critical embedded systems. Specifically:

- 25% reduction in integration costs
- 40% reduction in integration time
- 25% reduction of the efforts for integration tests
- 40% reduction of the average length of iteration cycles

The SPEEDS design process will provide the following capabilities:

- Construction of early system prototypes during the design stage.
- Thorough quality and stability assessment at early design stages.
- Active treatment of design assumptions to guide system development.
- Support for concurrent multi-organization development of complex designs.

The results from SPEEDS when applied to a new product design are expected to achieve an overall 60% reduction of costs for development and use of embedded systems and a 40% reduction of development time and to have an impact on product life costs by reducing the costs from recalls and/or catastrophic failures by 40% and reduce certification costs for avionics by 50%. My preference is for text here not bullets.

The partners maintain that they are pioneering new approach to systems engineering to minimise the risk to concurrent design activities by means of a new tool supported process. The process allows designers to establish rich component models that support functional and non-functional aspects. Appropriate models are then to be integrated as components in the construction of complete virtual models early in the design process. The aim is to derive efficient implementations from abstract models.

The process introduces novel formal analysis tools and techniques to assess the properties of a system precisely and allow the designer to explore alternative hardware and software architectures. The aim is

to achieve correct-by-construction design that allows scalability for large systems through compositionality and abstractions.

The partners have a plan for industrial pilot projects in the automotive and aerospace domains.

HIJA

High-Integrity Java Application

STREP, Project dates: Start 06/04 End 08/06

Introduction

In order to deliver a new generation of high-integrity real time applications, a more flexible, architecturally neutral implementation strategy is needed. The key to providing this flexibility is the development of architecturally neutral, real-time middleware technologies that support high-integrity systems.

Objectives

The HIJA project created a new Java based real-time middleware platform that supports the development of architecturally neutral, high-integrity real-time systems (ANRTS). These high-integrity embedded systems can have both hard and soft timing constraints and can be designed for safety-critical as well as business critical and ambient intelligence applications. Their design, maintenance, and certification require highly flexible, hardware independent technology to ensure cost effectiveness. The ANRTS research and technology development in HIJA addressed: identification of suitable computational models, analysis techniques and tools for ensuring functional correctness, advances in real-time resource usage and schedulability, reference implementations including native code, partitioning, and predictable memory management, real-time networked applications support including units of distribution and an approach to dynamic code replacement. This is used with a development process support based on Java program annotations that provide traceability, source level debugging, and run-time monitoring.

Results

The HIJA project has provided embedded systems developers the capability of dynamic deployment and code portability? in high integrity systems. Through the extension of Java's "write once, run anywhere" features, it is possible to provide portability and upgradeability for a wide range of embedded applications. These results will provide benefits for the embedded systems industry including:

- Increased developer productivity over current hardware-specific programming methods.
- Substantial savings in migrating embedded systems to different processor architectures
- Reductions in maintenance costs for embedded systems applications.

The partners developed 3 Profiles of Real Time System Java (RTSJ) as different products need different levels of assurance and the full RTSJ is overly complex for some applications.

- **HRTJ** Profile: Hard Real-Time Java, aimed at safety- and mission-critical apps
- **SRTJ** Profile: Soft Real-Time Java, aimed at mission- and business-critical apps
- **FRTJ** Profile: Flexible Real-Time Java, aimed at business critical apps including future ambient intelligent apps

The HIJA project has contributed to standards development activities for safety-critical Java, mission-critical Java, and the ARINC 653 Part 2 extensions of the Aerospace safety standards. The HIJA developments are suitable for safety-critical systems (e.g. aviation and automotive), business-critical systems (e.g. production and real-time resource management) and flexible dynamic systems (e.g. smart houses and learning).

ICODES

Interface- and COmmunication based Design of Embedded Systems

STREP, Project dates: Start 08/04 End 11/07

Objectives

The main target of ICODES was to provide a design technology for embedded systems with many communicating components in hardware and software. A methodology to model, evaluate and implement embedded hardware/software systems from the specification at Electronic System Level (ESL) to a standard industrial back-end design flow was developed. The ICODES tool flow defined a

Embedded Systems Design Workshop 08/04/08

system specification language based on SystemC 2.0. Techniques like communication based design and object-orientation are integrated into a seamless design flow for embedded systems. This supports analysis and optimisation of the system's communication properties. The tool set includes analysis, simulation, optimisation, and synthesis tools supporting interactive design decisions as well as the automatic translation and optimisation of transaction level SystemC models into HDL and C/C++ based implementations. An integrated development environment (IDE) ensures the seamless integration of these tools and of the design flow.

Results

Abstract design modelling at transaction level allows abstract Read/Write, generation of heterogeneous communication components, HW interface module generation, SW interface routine generation, generation of HW-buses, the binding of modules to existing system buses. This high level modelling allows for the HW/SW partitioning not to be decided until design synthesis. The automated generation of interfaces and communication channels gives benefits from being faster than manual implementation and being less error-prone. The advantages of the ICODES design flow stem from raising the level of abstraction to transaction level modelling of high level design elements, the development of analysis and modelling frameworks for system design and the development of a synthesis framework from transaction level to hardware description language (VHDL). This reduces the size of the step function change to the development process.

The industrial partners in the project demonstrated the usefulness of the tools and methods on industrial demonstrators including an automotive night vision video system and JPEG 2000 applications. The work on demonstrators highlighted the need for further developments to address:

- Software-to-software communication
- Communication topology
- Transparency of communication partners: HW or SW
- Communication timing
- Blocking behaviour
- Bus loading

VERTIGO

Verification and Validation of Embedded System Design Workbench

STREP, Project dates: Start 06/06 End 12/08

Introduction

VERTIGO deals with the development of technologies and tools to integrate verification of embedded systems built upon configurable platforms, within economical and technical constraints. Simulation to the automotive grade "safety" standard requires improved coverage which demands faster simulation with proper fault/error models at transaction level. VERTIGO exploits the results and tools coming from the IST-FP5 SYMBAD project and widens the spectrum of formal techniques applied at the verification of embedded systems.

Objectives

The main target of VERTIGO is to reduce the verification time of embedded systems built on configurable platforms by narrowing the gap between the Transactional Level (TL), that is becoming popular for system level modelling, and the HDL based RT level, that represents the entry for the physical implementation. A major effort in VERTIGO is to integrate dynamic and static verification around an assertion based approach. Static techniques will be analysed in the context of Petri nets and High Level Decision Diagrams (HLDD) in addition to the proven SAT solver approach. The extension of the SYMBAD Property Coverage Checker (PCC) concept will be considered to serve as a framework for collecting common coverage figures.

Several formal techniques will be investigated that can contribute to different stages of the design flow; modelling and verification (SW, TLM, RTL, module, system) and integrated with the simulation-based approach (dynamic verification). An Assertion Based Verification (ABV) method will be developed, that can be used both in static and dynamic verification with emphasis on TLM. A SW/HW co-verification environment will be prototyped.

Results to date

The technologies investigated in VERTIGO have improved the performance of the target Industry Workbench through the successful integration of technologies from the EDA tools developed by the SME partners. This is now being used in an industry product group.

The SME partners have benefited from having an industry driver to benchmark SME tools and the university partners have gained from having their technologies included in SME products. The SMEs will benefit from having industrial-grade products that increase credibility with other industry customers and co-operation with major EDA vendors.

COMPARE²

COMPonent Approach for **Real-time** and **Embedded**

STREP, Project dates: Start 06/04 End 12/07

Introduction

A general trend in software for real-time and embedded systems is towards complexity. This is due to the increased functionality these systems are required to support as well as to the fact that they are now often part of a more general system and are integrated in it. Traditional software had also to face this increase in complexity and had developed new paradigms to take it into account. A very promising one is the *component/container model (CCM)*. The CCM provides two fundamental features

- A component not only explicitly describes the services it provides but also the ones it requests to be provided by other components.
- A component is meant to be hosted by a container that takes into account the management of the technical properties provided by the underlying infrastructure, on the behalf of its components.

These features are key concepts to manage complexity and to allow effective reuse. CORBA has moved towards real-time and embedded areas. With the adoption of *Lightweight CCM*, CCM has started a move in the same direction by defining a minimum profile upon which it is now possible to build a model dedicated to real-time and embedded software

Objectives

- The goal of the project was to define a framework for RT/E systems, adapting the CCM for that purpose, to develop a reference implementation, to assess it on two case studies and to promote the definition to standardisation (OMG).

Results

- The definition of a RT/E framework based on Lightweight-CCM;
- A reference implementation on top of RTCORBA;
- A first use-case built with the reference implementation (Software Radio domain);
- A derived partial implementation on top of OSEK-VDX;

These results are accompanied by dissemination and exploitation activities with the goal to derive products from the achieved results and to market them.

INTEREST³

INTegrating **EuR**ocean **Embedded** Systems **T**ools

STREP, Project dates: Start 07/06 End 07/08

Introduction

The project INTEREST aims to overcome the current lack of integration and interoperability of tools for developing Embedded Systems software. The partners in the proposed project comprise a group of European tool vendors that jointly address the Embedded Systems Design flow. The following capabilities are targeted:

- Mapping of a logical architecture, i.e. the structure of the control-algorithms, to a technical architecture,
- Analysis of timing-related objectives for system and nodes
- Tool integration along the “V” development cycle, spanning all the analysis, system design, module design, implementation (including certified code generation), functional testing, module testing, system testing and requirements testing

² The project COMPARE has not been presented at this workshop, but is included as one of the FP6 projects on Embedded Systems Design from call 2.

³ The project INTEREST has not been presented at this workshop, but is included as one of the FP6 projects on Embedded Systems Design from call 2.

Objectives

The project aims to create techniques for improved interoperability (the INTEREST development framework) among European Embedded Systems Design, code generation, and verification COTS (commercial off the shelf) tools, which had not previously been achieved:

- SCADE from ESTEREL TECHNOLOGIES
- ASCET and INTECRIO from ETAS
- DESIGNER Pro from DECOMSYS,
- Dependable COTS code (such as UNIS hardware abstraction layer COTS)

The project will develop novel techniques for system-level and node-level analysis of non-functional properties, such as worst case execution timing, stack usage and schedulability analysis. These Analysis tools from ABSINT, EVIDENCE and SYMTAVISION will be then integrated into the INTEREST development framework. The INTEREST framework will contribute to further securing Europe's position of independence in Embedded Systems.

Expected Results

The overarching objectives of INTEREST are to reduce the time for the integrated development of embedded systems and the cost of development of these systems. In a period of five years after project start, the partners expect to achieve a reduction of 80% or more of the cost of performing mapping and timing analysis tasks within a typical Embedded Systems Design project.

During the project timeframe there will be demonstrators from within the aerospace and automotive application domains of the achievement of the quantitative objectives that will show the clear path to the overarching objectives:

- 50% time gain in timing analysis
- 50% gain in mapping time and significant improvement of mapping quality (equal or better quality in half time)

MOGENTES⁴

Model-based GENeration of Tests for Embedded Systems.

STREP, Project dates: Start 01/08 End 12/10

This new FP7 project has objectives to significantly enhance testing and verification of dependable embedded systems by means of automated generation of **efficient** test cases that rely on the development of new approaches as well as innovative integration of state-of-the-art techniques. The project has the goal to **reduce testing effort by at least 20%**.

The project plans to address both testing of functional safety tests and non-functional issues like reliability, e.g. by system stress or overload tests and to apply these technologies in large industrial systems. The aim is to be able to allow application domain experts (with little knowledge and experience in usage of formal methods) to use them with minimal learning effort.

The aspects to be considered are:

- Common modelling languages and semantics for domain specific requirements and (partial) models of the demonstrators
- Test theories to show conformance in the relationship between the model and implementation and to explore the notion of success and failure of a test case.
- Fault models will be enhanced by extending modelling languages
- Coverage criteria
- Model-based fault injection (MBFI) to validate the defined fault models (and thus the generated test cases) with physical fault injection
- Design system framework to enable semantics-aware transformations from system models to inputs of specific tools and to interface with existing simulation/test environments from industrial partners

There will be application demonstrators with examples taken from automotive, off-highway vehicles and railway interlocking

⁴ The project MOGENTES from FP7 call 1 has been presented at this workshop, as it was represented by the same person as the FP6 project DECOS.

Recent and forthcoming calls for proposals

FP7 Call 1, objective 3.3, Embedded Systems Design, Budget: 40 M€

Target Outcomes:

- 3.3.a) Theory and methods for system design: STREP and NoE
- 3.3.b) Suites of interoperable design tools for rapid design and prototyping:
 - Interoperable tools from SMEs: STREP and CSA
 - Tool developer's RTD work: IP
 - Open tool frameworks: STREP and CSA
- 3.3.c) Coordination of national, regional and EU-wide R&D programmes
CSA

The coverage of the objectives by these projects is shown on the presentation slide 3.

Future Orientations in Embedded Systems Design

R&D work is required to match the increasing complexity demand with increased system design productivity supported by efforts to inspire the emergence and growth of embedded systems tool vendors.

ARTEMIS Joint Undertaking

Call 1 : Sept 2008 (Budget ~97 M€ from EC and MS)

- Methods and Processes for Safety-relevant Embedded Systems (high priority)
- Person-centric Health Management
- Smart Environments and Scalable Digital Services (high priority)
- Efficient Manufacturing and Logistics
- Computing Environments for Embedded Systems (high priority)
- Security, Privacy and Dependability in Embedded Systems for Appliances/Networks/Services
- Embedded Technology for Sustainable Urban Life
- Human-centric Design of Embedded Systems

FP7 ICT Target outcomes WP '09-10, Objective 3.4 (Budget 28 M€) :

- a) Theory and novel methods for system design
- b) Modules and tools for embedded platform-based design
 - Increased interoperability of tools and openness
 - Efficient resource management
 - Design space exploration
 - Advanced model-driven development
 - Emergence and growth of embedded systems tool vendors

Discussion of the presentations

Discussion of the presentation of the Network of Excellence

The successes of the NoE has been the creation of a fertile ground for the take up of new methods by giving young engineers in Embedded Systems the awareness of the emerging new methods and tools. There are many new tools, but these are not connected. Prototypes will not be used by industry, as they are not integrated in an end-to-end tool chain and not reliable enough. There is a need to further build on the work of the IP and STREPs projects in researching the methods and tools for end-to-end tool chains. The ARTIST2 NoE shows the strength of Europe in Embedded Systems Design with a good cluster of topics and the staffing of them with high quality researchers under the leadership of recognised experts. Whilst it was clear how the cluster domains had been managed it was said that there had been no formal programme of interaction between the cluster domains as the differences were too great.

The discussion re-enforced the widely held view that the domain of embedded systems and, in particular, the domain of Embedded Systems Design is very fragmented, there is a wide range of application areas to be covered and a wide range of product regulatory regimes to be met.

This difference between the applications areas is portrayed in the lack of penetration and adoption of ideas from other domains over many years. This had not been helped by the fact that the commercial solutions are from suppliers with their own agendas driven more from the s/w engineering aspect.

It was agreed that the big difference in maturity and support between research tools and industrial tools leads users not to trust research tools and thus not try out the new methods that are supported by research tools. The trust in new methods would only come from having methods and tools shown to be validated on industrial cases and the role of Framework Projects in facilitating industry to take on these risks is key to achieving this trust.

It was proposed that the consumer application area is the most likely to start the take up of ideas from other areas as consumer is more under pressure and is less bound by the constraints imposed by product regulatory regimes and issues of civil liabilities that apply to the aerospace, automotive and avionics domains.

In summary the successes of ARTIST2 are:

- Branding of the NoE and its association with the Embedded System domain.
- Creation of a closely-knit research community.
- Creation of the infrastructure (workshops, events, schools ...) for the research community.
- Development of the scientific agenda for Embedded Systems research.

The NoE has made some progress in establishing Embedded Systems as a discipline, but there are no dedicated full-time degree courses as yet. Students from the universities do not learn system engineering. It was suggested that the NoE could extend its scope to have a major role on curricula definition for full-time degree courses to help achieve the necessary mentality change in future engineers. This should become a topic for the successor NoE, ArtistDesign.

One of the successes of ARTIST2 has been the spawning of new project proposals. There is a significant point for potential improvement possible in the consortium building process. This could become more efficient and result in more effective consortia. The hardest part of consortium building is getting the involvement of the product development, rather than the research, groups of the industrial partners. There is a natural reluctance to risk a development by using new (to them) methods even though there are potential gains in productivity, product quality and reduced development costs. It was suggested that workshops are run aimed at the Chief Technology Officers of companies to educate in the benefits of new methods resulting from research into Embedded System Design. Success in this endeavour would open up the possibility of more rapid take up of results and engagement of product developers in the project consortia.

Discussion of the presentations of the Integrated Projects

Although the foundation of the 3 IP projects was different:

DECOS	Time triggered systems
ASSERT	Proof based system design
SPEEDS	A process of contracts and relationships between components,

each of the projects had a common theme to raise the level of abstraction of design and modelling and produce an end-to-end tool flow that satisfied their requirements. The use of higher level of abstraction modelling raises the productivity in development but raises the issue of keeping the semantics of the design when transferring data from one model to another and from one technique to another. There was a general agreement that automating the transformations from one level of model to another level of model is the solution to maintain the design semantics.

The value of abstraction of design to higher levels has a clear productivity gain. However the development of methods from different problem bases will lead to a plethora of solutions and this leads to standardisation becoming even more important. The users must drive the push for standardisation.

The key question in the evaluation of these projects is how the results have been exploited by the partners and by third parties outside the consortium. How are things different today after these 3 IP projects, especially in the context of industrial take up?

This was felt to be a difficult question to answer, as it was stated that, in some companies and institutes, there are now policies not to use internal tools. Obviously tool providers mainly exploit outside the consortium. Openness and standardisation is crucial, as a company will not invest when only one tool vendor is offering a new tool or method. The big winner in both the ASSERT and DECOS projects was the SME partner.

With DECOS outcomes, the SMEs Esterel Technologies (F) and TTTech (A) improved and expanded their product palettes and Profactor (A) gained experience in critical vibration suppression using timer-triggered technologies. Furthermore, in Hungary a new SME OptXware (Spin-off from Budapest University of Technology and Economics) has been founded for exploitation of DECOS results concerning model-based safety-critical application development using model transformations.

Discussion of the presentations of the STREP Projects

Where are we today compared with the position 3 years ago:

- Has the Embedded System Design problem become more complicated?
- What are the biggest evolutionary steps to have taken place?

It was agreed that the problem of Embedded System Design has become much more complicated with the drive to exploit the latest technologies and to combine what would have been multiple separate embedded systems into a federated system platform. The biggest forward step is the use of higher level modelling like UML, but the tools are complex and open to being misunderstood and to be used in less than an optimum way. It was suggested that the Object Oriented approach is an example of this effect.

There is a need for domain specific modelling methods and tools, as an example; Simulink is a useful tool for control engineers as there are specific notations for the various domains of Embedded Systems Design. This raised the point that there is opportunity for work to develop domain specific front ends to the commonly used general purpose tools along the same lines as the provision of domain specific toolboxes for Simulink/MATLAB.

There is a good benefit to be across the industry from adoption of new methods and it was suggested that a scale to measure this value can be understood by likening a major aerospace ground systems to a major commercial banking systems.

It was generally agreed that there is a pressing need for a catalogue of project results, what they do and who is responsible for making them available and supporting them. It was suggested that the NoE is in a position to do this however the NoE is not necessarily motivated or staffed to this end.

Conclusions and Recommendations

The aim of this evaluation workshop was to provide feedback on how the programme objectives have been realised, to use evaluation results to adjust programmes and to review the relevance of the programme.

Conclusions

The FP6 & 7 programmes have been, and remain, highly relevant to the key objective of enabling Europe to retain the pre-eminent position it has in Embedded Systems. There is documented evidence [OECD] to show that other countries have made R&D investment to try to close the gap, this must cause Europe to strengthen its efforts to maintain the leading position. There is evidence from the USA that they see the need for educational changes to consider Embedded Systems (or Cyber-Physical Systems) as an engineering discipline in its own right. The NoE projects have achieved good results in creating the needed community for Embedded Systems Design and development, in setting the research agenda and spawning new project proposals for R&D work to address the designer productivity issues described below. Future opportunities exist for developing the curricula for specific Embedded Systems degree courses. The R&D projects commissioned by the FP6 and FP7 programmes of work have met their stated objectives with the development of end-to end design systems and middleware. These achievements show productivity gains in application software and in the development of hardware by raising the abstraction level of design and where appropriate the project partners have promoted their developments into the standards applicable to their domain of work. The progress to date is just one step in the overall objective of enabling Europe to retain the pre-eminent position it has in Embedded Systems. Continued investment in a sustained programme of research and development in design methods for Embedded Systems and in education to bring about the cultural change from Embedded System design being considered largely a craft based process to becoming a science based industrial process is needed. To this end, the Framework supported R&D projects and Networks of Excellence and the function of the ARTEMIS technology platform and its supporting association ARTEMISIA, must continue the work to create an identity and a focus to bring about the cultural and methodological changes in the community of Embedded Systems.

Technology productivity increases according to Moore's Law that is approximately 2X increase in device integration capability every 1½years. The designers' ability to design chips and applications software lags behind this rate of increase and has been increasing at the rate of 2X every 4 to 5 years. This results in a disproportionate increase in the size of the hardware design teams and the application development teams for embedded systems with the attendant escalation of cost. Efforts to devise methodologies and tools to increase designer productivity, both hardware and software, are essential to maintain Europe's leading position in the design and implementation of embedded systems. The progress of the semiconductor industry will continue unabated for the foreseeable future, therefore the existing design gaps for hardware and software will widen unless there are significant efforts to improve designer productivity.

The discussions re-enforced the widely held view that the domain of embedded systems and, in particular, the domain of Embedded Systems Design is very fragmented because there is a wide range of application areas and a wide range of product regulatory regimes to be met. This difference between the applications areas is demonstrated in the lack of penetration and adoption of ideas from other domains over many years. The big difference in maturity and support between research tools and industrial tools leads users not to trust research tools and thus not try out the new methods that are supported by research tools. The trust in new methods would only come from having methods and tools shown to be validated on industrial cases and the role of Framework Projects in facilitating industry to take on these risks is key to achieving this trust.

The take up of existing results outside the project partners seems slow. The market for software application development tools is much greater than that for the corresponding hardware development tools but has not taken off in the same way. The parallel market for the hardware development is more tightly constrained by the manufacturing processes used to realise hardware. Whilst it is clear that there are committed tool vendor partners in the projects with a clear intent to sell on the tools generated in the projects, all the presenters at this workshop agreed that the tools market for embedded application software development is a difficult and fragmented market characterised by the diverse application areas and the context specific notations that persist from the culture of the various industries. Amongst the factors contributing to the perceived market failure suggested was the wide range of applications, the wide range of the composition and maturity of development teams, the wide range of product regulatory regimes to be satisfied and the lifetimes of tools and tool companies (for continues assured

support) when compared with the projected product lifetimes for aerospace, telecoms infrastructure, avionics and automotive products which range from 10-30+ years.

Where other software development tools are migrating to the model of an Open Source repository, the regulatory requirements for many embedded applications would seem to preclude this happening in this area, as there is no guarantee of support, no assurance of performance and no audit trail of ownership for liability issues.

Selling integrated tools into a market that is fragmented is clearly an issue for tool vendors. Engagement of tool vendors in FP projects can lead to early commitment from prospective customers and would expose tools companies to the rationale of the requirements for long term support of users.

Recommendations

1. Continue with Networks of Excellence.
2. Seek to improve designer productivity.
 - a. research and development into new methods of product specification and supporting tools for concurrent engineering of the application software alongside the hardware development
 - b. software reuse, openness
 - c. integrated end-to-end design environments
 - d. develop methods and tools for higher levels of abstraction.
 - e. methods for software-to-software communication
 - f. communication topology
 1. transparency of communication partners,
 2. communication timing
 3. blocking behaviours
3. Supporting Action for cataloguing project results, what they do and who is responsible for making them available and supporting them.
4. Develop domain specific front ends to the commonly used general purpose tools.[Now that this is more emphasised on the discussions section maybe we can shorten the text of the recommendation by removing the reference to the example of Simulink/MATLAB here][There is a reference in the text. I have highlighted it in yellow and added the MATLAB example there too.]
5. Promote standardisation of common methodologies.
6. Encourage wider participation of tools companies, large and small within R&D projects.

Annex A: References

Citations

- [Henzinger & Sifakis] The Discipline of Embedded System Design, IEEE Computer Oct 2007
[OECD] OECD Science, Technology and Industry Scoreboard 2007
[IST-WP0307] Information Society Technologies, 2003-2004 Work Programme, ISBN 92-894-4092-9, Office for Official Publications of the European Communities, 2003
- [ARTEMIS] Artemis Strategic Research Agenda 2006.
[FAST] Study of Worldwide Trends and R&D Programmes in Embedded Systems. European Commission, Report, 2005

Sources of further information

Website of the Workshop:

http://cordis.europa.eu/fp7/ict/esd/events-20080408_en.html

Portfolio of DG INFSO Embedded Systems and Control Unit:

<http://cordis.europa.eu/ist/embedded/projects.htm>

Websites of the projects:

[Artist2 - http://www.artist-embedded.org](http://www.artist-embedded.org)

[ASSERT - http://www.assert-online.net](http://www.assert-online.net)

[DECOS - http://www.decos.at](http://www.decos.at)

[SPEEDS - http://www.speeds.eu.com](http://www.speeds.eu.com)

[HIJA - http://hija.info](http://hija.info)

[ICODES - http://icodes.offis.de](http://icodes.offis.de)

[VERTIGO - http://www.vertigo-project.eu](http://www.vertigo-project.eu)

[MOGENTES - http://www.mogentes.eu](http://www.mogentes.eu)

Annex B: Attendees and Agenda

Workshop Attendees:

Konstantinos Glinos, HoU, DG INFSO Embedded Systems (G3)
Alkis Konstantellos, Deputy HoU (G3)
Gisele Roesems-Kerremans, Deputy HoU DG INFSO Nanoelectronics (G1)
Philippe Reynaert, DG INFSO (G3)
João Sousa, DG INFSO (G3)
Jean-François Buggenhout, DG INFSO (G1)

Bruno Bouyssounouse, VERIMAG..... ARTIST2
Eric Conquet, ESA ASSERT
Wolfgang Herzner, ARCS.....DECOS & MOGENTES
Drora Goshen, IAI..... SPEEDS
Antonio Kung, TRIALOG..... HIJA
Andreas Schallenberg, OFFIS/University of Oldenburg ICODES
Andre Vandemeulebroecke, STM VERTIGO

Rapporteur: Jim Heaton, JH Associates Ltd

Workshop Agenda

08:30 Registration
09:00 Opening
 Konstantinos Glinos
09:15 Presentations (NoE)
 ARTIST2, Bruno Bouyssounouse
10:00 Discussion
10:45 Coffee break
11:00 Presentations (IPs)
 ASSERT, Eric Conquet
 DECOS, Wolfgang Herzner
 SPEEDS, Drora Goshen
12:00 Discussion

12:45 Lunch

14:00 Presentations (STREPs)
 HIJA, Antonio Kung
 ICODES, Andreas Schallenberg
 VERTIGO, Andre Vandemeulebroecke
15:15 Discussion
15:45 Coffee break
16:00 FP7 Call 1 and future calls
 Philippe Reynaert
 MOGENTES, Wolfgang Herzner
16:30 Discussion
17:00 Summary
 Jim Heaton
17:15 Closing